Amendments to the Drawings:

The attached replacement sheet of drawing includes changes to Fig. 2 and replaces the original sheet including Fig. 2.

In Figure 2, the legend --Prior Art-- was added.

Attachments following last page of this Amendment:

Replacement Sheet (1 page)

Annotated Sheet Showing Change(s) (1 page)

REMARKS

Claims 1-15 and 23-37 were pending as of the office action mailed on December 27, 2006. No new matter has been added. Applicant respectfully requests reconsideration in view of the following remarks.

**I. Drawing Objections**

The Examiner objects to the drawings, suggesting that Fig. 2 should be designated by a legend such as --Prior art--. Applicant has amended Fig. 2 as requested by the Examiner. No new matter has been added.

**II. Claim Rejections under 35 U.S.C. § 102**

The Examiner rejected claims 1, 3, 5-6, 11-14, 23-25, 27-28, and 33-36 under 35 U.S.C. § 102(b) as allegedly anticipated by U.S. Patent No. 6,898,722 ("Anzai"). Applicant respectfully traverses the rejection.

**a. Claim 1 and its dependent claims**

Claim 1 is directed to a circuit including a clock transmitter in communication with a clock bus, a clock receiver in communication with the clock bus, and a driver in communication with the clock bus. The clock transmitter transmits a clock signal on the clock bus. The clock receiver receives a clock signal on the clock bus. The driver drives and maintains a voltage of the clock bus to a first voltage level while the clock transmitter is not transmitting a clock signal on the clock bus and the clock receiver is not receiving a clock signal on the clock bus.

The Examiner suggests that Anzai shows the limitations of claim 1. Applicant respectfully disagrees. Applicant respectfully asserts that Anzai fails to teach or suggest, at least, a driver to drive and maintain a voltage of the clock bus to a first voltage level while the clock transmitter is not transmitting a clock signal on the clock bus and the clock receiver is not receiving a clock signal on the clock bus.

The Examiner suggests that Anzai's output circuit is Applicant's claimed driver and that Anzai's transfer clock 'c' (signal (L) in Fig. 5) is Applicant's claimed clock bus. As shown in Fig. 3, Anzai's output circuit takes as input a clock count value signal 'i' and an internal clock signal 'h' and generates a data output completion signal 'j'. (Col. 6, lines 32-33; Fig. 5).

Anzai's system transfers 8-bit data during a period equal to six clock pulses of the transfer clock. (Col. 5, lines 66-67). When the clock count reaches a value of six, indicating that the last bit of the 8-bit serial data has been transmitted, the output circuit generates a completion signal 'j'. (Col. 7, lines 26-30; col. 5, lines 52-54). The completion signal 'j' is then OR-ed with the internal clock signal 'h' to generate Anzai's transfer clock signal 'c'. (Col. 6, lines 35-37). As shown in Figs. 2 and 5, the OR operation causes the transfer clock signal 'c' to go high "during a period from the leading edge to the trailing edge of the odd-numbered data." (Col. 59-61). After this period (i.e., after the completion signal terminates) the transfer clock floats low. (Figs. 2, 5). Anzai's sending unit transmits the transfer clock signal 'c' via output terminal 115 to input 203 of Anzai's receiving unit. (Col. 6, lines 36-37, 43-45; Fig. 4).

Applicant respectfully asserts that Anzai fails to teach or suggest, at least, a driver to drive and maintain a voltage of the clock bus to a first voltage level while the clock transmitter is not transmitting a clock signal on the clock bus. The Examiner suggests that Anzai's transfer clock signal 'c' is Applicant's claimed clock bus. However, Anzai's transfer clock signal 'c' is maintained at *two different levels* after data transmission completes: the signal is held high for the duration of the completion signal, and floats low after the completion signal terminates. (Fig. 2, 5; col. 5, lines 59-65). Applicant respectfully asserts that Anzai's ~~The~~ high state of transfer clock signal 'c' is not Applicant's claimed first voltage level *while the clock transmitter is not transmitting a clock signal* on the clock bus, because the clock transmitter is transmitting clock signals during this segment: system clock 'd' is continuously transmitting, and internal clock 'h' continues transmitting a clock signal until the falling edge of transfer clock signal 'c'. (Fig. 5). Additionally, the floating state of transfer clock signal 'c' is not Applicant's claimed first voltage level. After the completion signal terminates, transfer clock signal 'c' transitions low and floats - Anzai does not indicate that the signal is maintained at *any* particular voltage level. (Fig. 5). Finally, transfer clock signal 'c' is certainly not driven and maintained to a first voltage level when the signal is viewed in its entirety. As discussed above, transfer clock signal 'c' is held at multiple levels, i.e., a high state and a low floating state. In fact, Anzai's design *requires* these

multiple levels, because it is the high-to-low transition that indicates to the receiving unit that data transmission is complete. (Col. 5, lines 54-65).

The Examiner rejected claim 1, stating that Anzai's output circuit was a driver to drive and maintain "a voltage [e.g., low after completion signal] of the clock bus to a first voltage level [associated with completion signal]." It is unclear whether the Examiner means to suggest that Applicant's first voltage level is the high voltage found in Anzai (i.e., associated with the completion signal) or the low voltage (after the completion signal terminates). However, the very fact that this ambiguity exists demonstrates that Anzai fails to show a driver to drive *and maintain* a voltage of the clock bus to a *first voltage level*: Anzai's output circuit maintains the transfer clock at not one, but *two* different voltage levels. Applicant respectfully submits that claim 1 is allowable for at least these reasons.

Claims 3, 5-6 and 11-14 depend from claim 1, and are allowable for at least the reasons set forth above with respect to claim 1.

**b. Claim 23 and its dependent claims**

Claim 23 is directed to a circuit including a clock signal transmission means in communication with a clock bus, a clock signal receiving means in communication with the clock bus, and a voltage driving means in communication with the clock bus. The clock signal transmission means transmits a clock signal on the clock bus. The clock signal receiving means receives a clock signal on the clock bus. The voltage driving means drives and maintains a voltage of the clock bus to a first voltage level while the clock signal transmission means is not transmitting a clock signal on the clock bus and the clock signal receiving means is not receiving a clock signal on the clock bus.

Claim 23 is allowable for at least the reasons set forth above with respect to claim 1.

Claims 24-25, 27-28, and 33-36 depend from claim 23, and are allowable for at least the reasons set forth above with respect to claim 23.

**III. Claim Rejections under 28 U.S.C. § 103**

The Examiner has not established that Anzai teaches or suggests every limitation of Applicant's claimed invention. In particular, as discussed above, Anzai fails to teach or suggest,

at least, a driver to drive and maintain a voltage of the clock bus to a first voltage level while the clock transmitter is not transmitting a clock signal on the clock bus and the clock receiver is not receiving a clock signal on the clock bus. The additional references cited by the Examiner do not cure this deficiency.

**a. Claims 2, 15, 24, and 37**

The Examiner rejected claims 2, 15, 24, and 37 under 28 U.S.C. § 103 as being unpatentable over Anzai. Applicant respectfully traverses this rejection.

Claims 2 and 15 depend from claim 1, and are allowable for at least the reasons given above with respect to claim 1.

Claims 24 and 37 depend from claim 23, and are allowable for at least the reasons given above with respect to claim 23.

**b. Claims 4 and 26**

The Examiner rejected claims 4 and 26 under 28 U.S.C. § 103 as being unpatentable over Anzai in view of U.S. Patent No. 5,732,249 ("Masuda"). Applicant respectfully traverses this rejection.

Claim 4 depends from claim 1, and is allowable for at least the reasons given above with respect to claim 1.

Claim 26 depends from claim 23, and is allowable for at least the reasons given above with respect to claim 23.

**c. Claims 7 and 29**

The Examiner rejected claims 7 and 29 under 28 U.S.C. § 103 as being unpatentable over Anzai in view of U.S. Patent No. 4, 344,127 ("McDaniel"). Applicant respectfully traverses this rejection.

Claim 7 depends from claim 1, and is allowable for at least the reasons given above with respect to claim 1.

Claim 29 depends from claim 23, and is allowable for at least the reasons given above with respect to claim 23.

**d. Claims 8-10 and 30-32**

The Examiner rejected claims 8-10 and 30-32 under 28 U.S.C. § 103 as being unpatentable over Anzai in view of U.S. Patent No. 5,355,468 ("Jeppesen"). Applicant respectfully traverses this rejection.

Claims 8-10 depend from claim 1, and are allowable for at least the reasons given above with respect to claim 1.

Claims 30-32 depend from claim 23, and are allowable for at least the reasons given above with respect to claim 23.

**IV. Conclusion**

By responding in the foregoing remarks only to particular positions taken by the Examiner, Applicant does not acquiesce with other positions taken by the Examiner that have not been explicitly addressed. In addition, Applicant's arguments for the patentability of a claim should not be understood as implying that no other reasons for the patentability of that claim exist.

No charges are believed to be due at this time. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 3-26-2007

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